

## A New Inverter Design For Facts Applications

<sup>1</sup>Hemlatha J N, Aswathy K S<sup>2</sup>

*Assistant: professor Department of Electrical And Electronics Engineering, RVCE , Bangalore*

**Abstract:**– FACTS is used to operate the transmission line at stable condition. A number of FACTS controllers and various schemes of operation are already proposed. But a still lot of scope is left in this development to make it more efficient in terms of voltage stress , switching losses and harmonic suppression .The scheme proposed here is used a SSSC based on a multilevel inverter to demonstrate the results. This inverter can produce the pulses with different width and magnitude , and the output almost resembles a sine wave.The output results are compared with conventional type of SSSC.The simulation of both proposed system and conventional system are given in this paper . The sample of voltage and current will be taken from the transmission line and is given to the processor to determine the angle of firing for the switching device.

**Keywords:**– Flexible AC Transmission System (FACTS) ,Static Synchronous Series Compensator (SSSC) , Multilevel inverter , Cascaded H Bridge.

### I. INTRODUCTION

In recent years power demand has increased substantially while the expansion of power generation and transmission has been severely limited due to limited resources and environmental restrictions .As a consequence some transmission lines are heavily loaded and the system stability becomes a power transfer limiting factor .Flexible AC Transmission System (FACTS) Controllers have been mainly used for solving various power system steady state control problems .[1,2]

In late 1980's Electric Power Research Institute (EPRI) formulated the vision of Flexible AC Transmission System(FACTS) in which various power electronics based controllers regulate power flow and transmission voltage and mitigate dynamic disturbances .Generally the main objective of FACTS are to increase the usable transmission capacity of lines and control power flow over the designated transmission routes. [2,3]

Recent studies reveal that FACTS controllers could be employed to enhance power system stability in addition to their main function of power flow control [1,3] .The literature shows an increasing interest in this subject for the last two decades , where the enhancement of system stability using FACTS controllers has been extensively investigated.

There are different types of FACTS controllers .Among which some major types are Static synchronous compensator (STATCOM) , Static synchronous series compensator (SSSC) , Unified power flow controller (UPFC) , Interline over flow controller (IPFC) [2] . The major component of these facts devices is a converter , and various types of converters have been already proposed . If we use a normal type inverter or a single level inverter then the output will be a square wave , which contains remarkable amount of harmonics [4]. Therefore in this proposed system multilevel inverters are used for harmonic reduction .

Among the existing multilevel inverters cascaded h bridge type is the most simple inverter . It can produce 5 levels using 8 switches , 7 levels using 12 switches, 9 levels with 16 switches and so on[3,5,6]. But it clearly reveals that an increase in level demands more number of switches . Thus the comment simplicity on CMLI is simply contradictory .Hence the focus was eyeing on a real solution to this problem , that is how to simplify the complex circuit .Then arise the concept of “switch reduction”.

This paper proposes a unique design of inverter with reduced number of switches which can use for FACTS controllers .The main objective is to reduce the number of switches used in the converter and hence to reduce the switching losses .This system is designed to compensate the active power in transmission line and maintain the voltage to be in phase with the line current or at reduced phase angle displacement. Harmonic presence will also be reduced at remarkable levels . Fig 1 shows the schematic block diagram of FACTS compensation system.

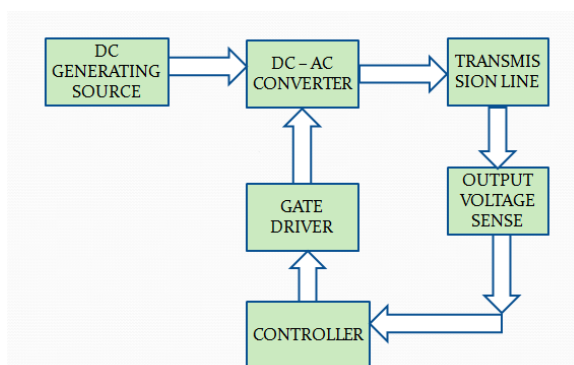


Fig 1 . Block diagram of a compensation scheme

## II. PROPOSED SYSTEM

In this paper in order to evaluate the results SSSC is selected ,and it is described in detail about the working principle and waveforms . In the proposed system DC voltage source will connected in series with the transmission line at various switching sequence depending on the PWM signals .[7,8]. PWM signals are generated based on the transmission grid voltage . Transmission voltage parameters are sensed by PT (Potential Transformer) and corresponding signals are given to the controller in which PWM generation is decided[9,10].

## III. PROPOSED INVERTER

Aiming at reducing the switches to the maximum possible extend and reducing complexity , the new topology is introduced with 8 switches for seven level. The new configuration is made with a special arrangement with 4 DC sources for 7 level.

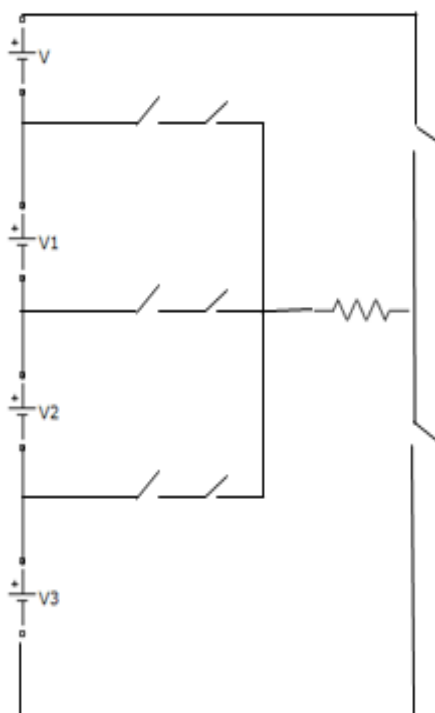


Fig2. Schematic diagram of the proposed topology

The less switches we use lessen the cost of circuit building .The circuit thus obtained is the simplest design compared to conventional cascade type inverters. For a seven level output cascade configuration needs 12 switches and 3 DC sources. Ofcourse this new design uses one extra DC source than conventional inverters. But moving on to the higher levels ,consider a 25 level , cascade inverter requires 12 DC sources and 48 switches [9] and using this new topology it is possible by using 13 DC sources and 28 switches. This great reduction in switches compensate the additional requirement of DC source.

#### IV. SWITCHING SCHEME

	S1,S6	S2,S7	S3,S8	S4	S5
+VDC	0	0	1	0	1
+2VDC	0	1	0	0	1
+3VDC	1	0	0	0	1
0	0	0	0	0	0
-VDC	1	0	0	1	0
-2VDC	0	1	0	1	0
-3VDC	0	0	1	1	0

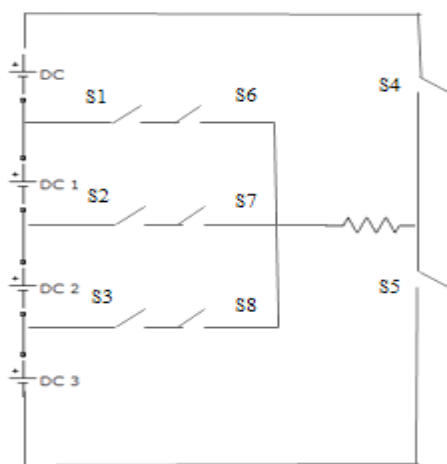
Fig 3.Switching Scheme For The Proposed Inverter

In this proposed topology only two switches S6 & S7 plays the role of polarity reversal. In other three positions to make the bidirectional conduction possible, two MOSFETs are used in series. These three positions need to be compulsory bidirectional or else the waveforms will get distorted. Reduced switches makes the circuit compact and user friendly. Though the usage of 4 DC sources for seven level results in less utilization of sources, switch reduction benefits in low switching loss.

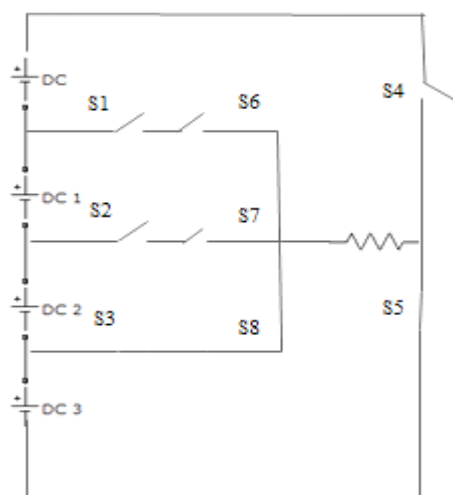
#### 5. MODES OF OPERATION

This inverter has 12 modes of operations to get the seven level output .Here explains some modes of operations of the proposed inverter. And the remaining modes can be manipulated from these.

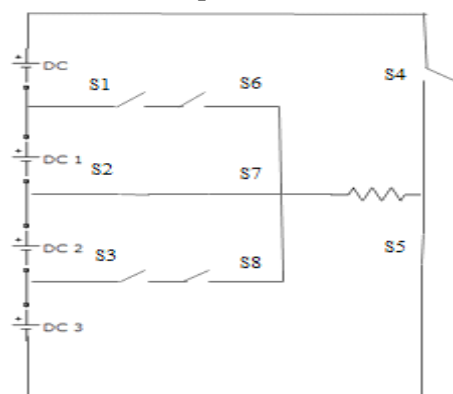
Output = 0



Output = +Vdc

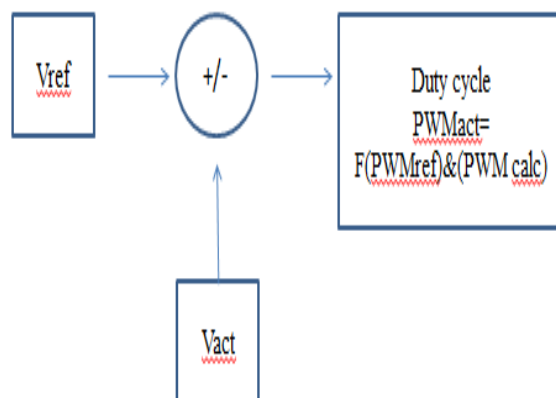


Output= -Vdc



## VI. VOLTAGE CONTROLLER

In the generation of PWM pulse , controller should monitor the transmission line parameters and depending on these parameters the duty cycle is decided. The actual voltage is taken from the transmission line and a reference voltage is set. Comparator combines the reference voltage and the actual voltage which results in change of duty cycle.



**Fig 4. Controller diagram.**

The above figure shows the controller diagram for the proposed system. Actual PWM value decided by comparing the calculated value and desired value. The calculation of duty cycle is as follows.

$$PWM \text{ calc} = (T_{on} / (T_{on} + T_{off}))$$

If  $V_{act} > V_{ref}$

$T_{on} = T_{on} - \text{Unit size}$  &  $T_{off} = T_{off} + \text{Unit size}$ .

If  $V_{act} < V_{ref}$

$T_{on} = T_{on} + \text{Unit size}$  &  $T_{off} = T_{off} - \text{Unit size}$

The unit size is the time range which generated based on the controller calculated value. If  $V_{act} = V_{ref}$  then duty cycle is maintained as it is.

### VIII. SIMULATION RESULTS

The simulation works for the proposed system is done with the help of SIMULINK in MATLAB. First the inverter alone is simulated and then the FACTS controller based on the new inverter. To compare the results both the SSSC schemes , conventional SSSC based on the cascaded H bridge scheme and new inverter topology based SSSC schemes are simulated .MOSFETS are used as switches. In most of the switching devices losses will be there . So the device selection has done based on switching losses.

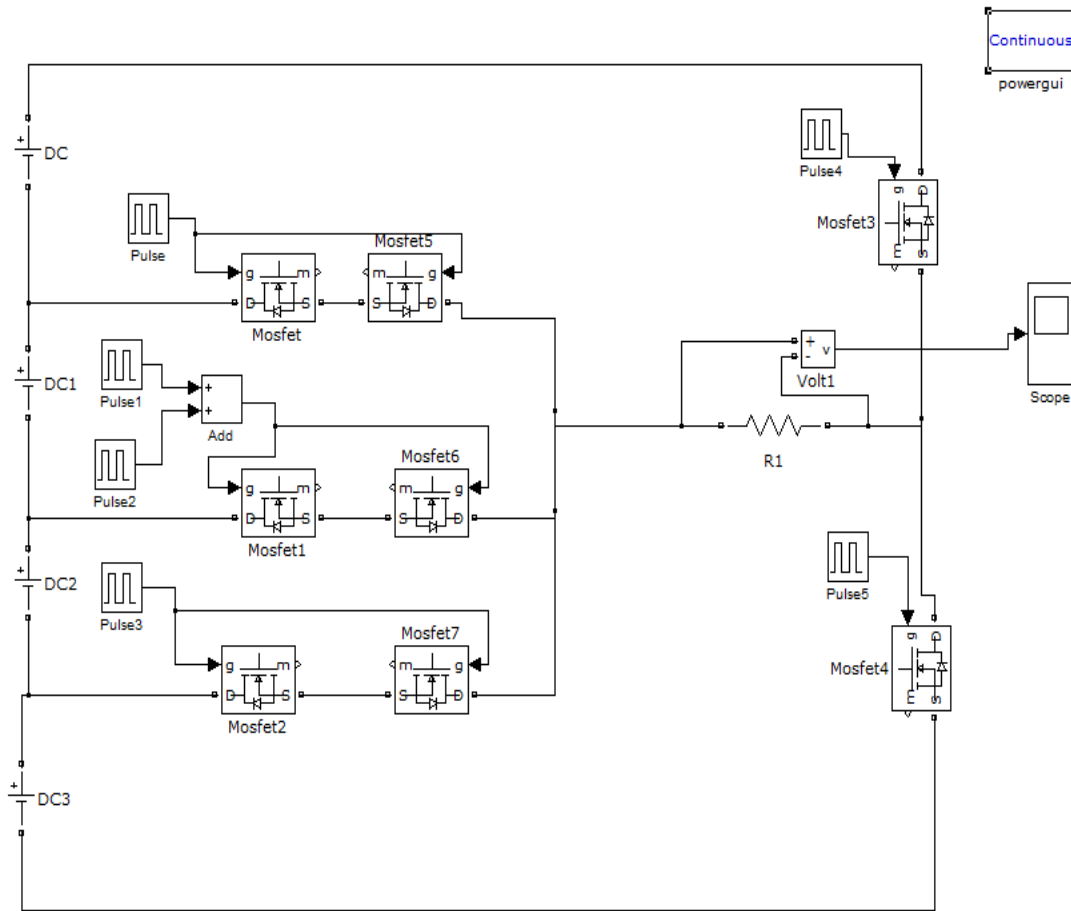


Fig 6 .Simulation diagram of the proposed inverter.

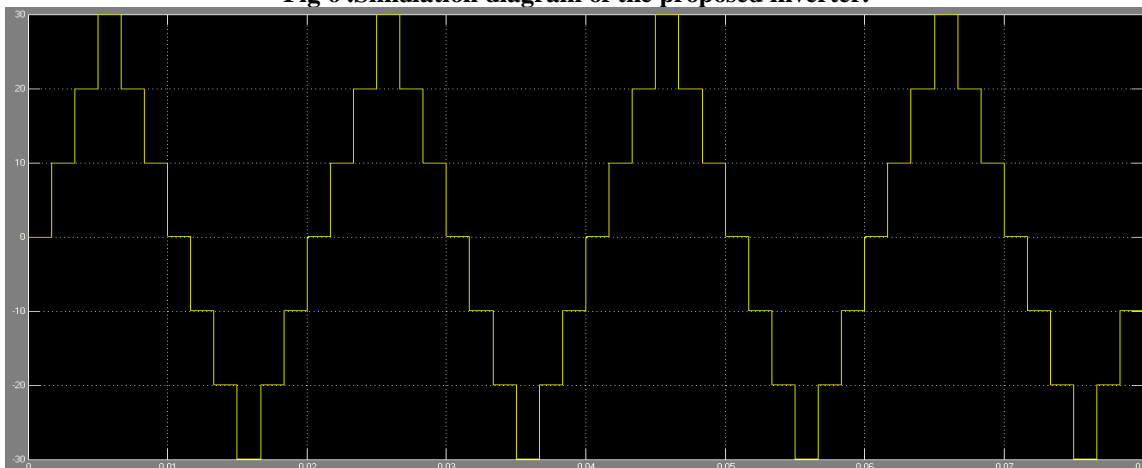


Fig 7 . Seven level output waveform.

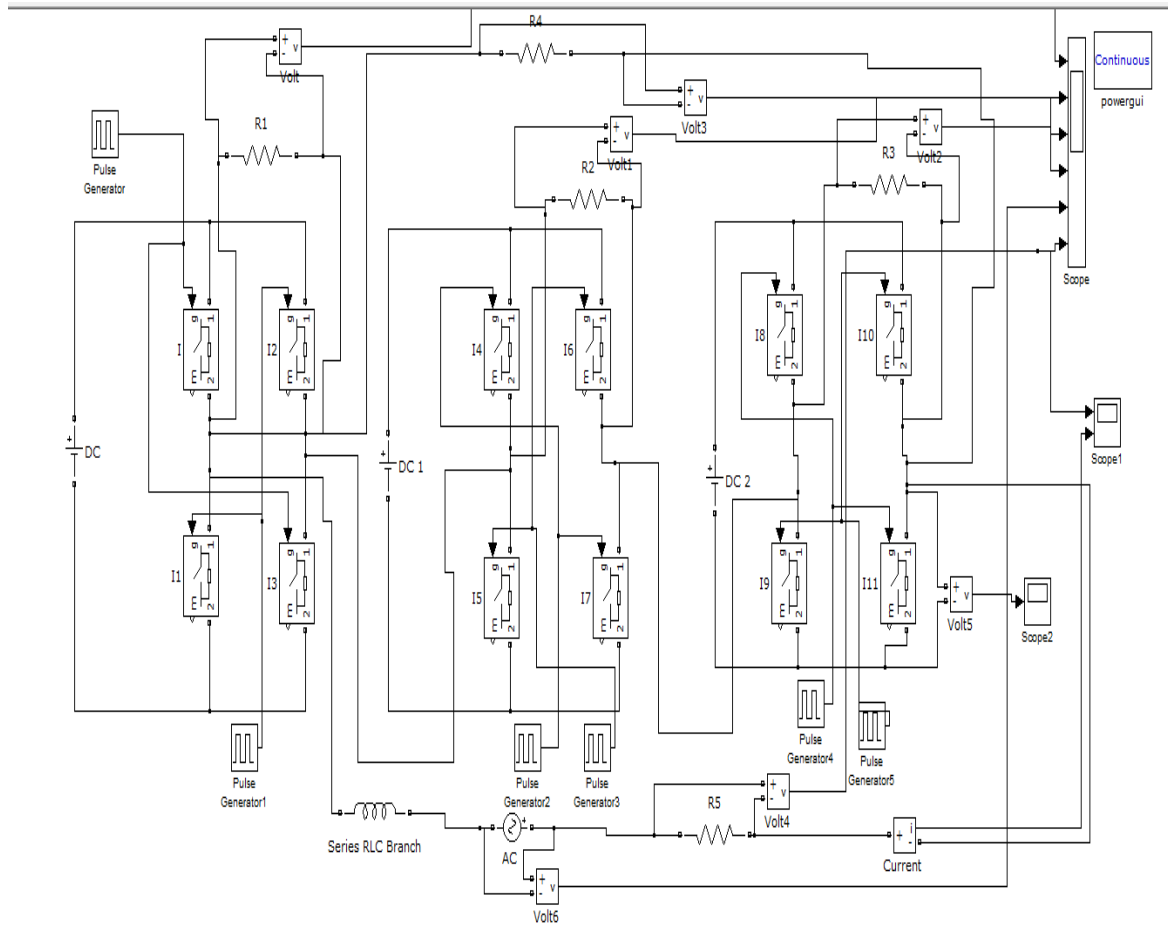


Fig 8 .Simulation diagram of SSSC based on cascaded H bridge inverter.

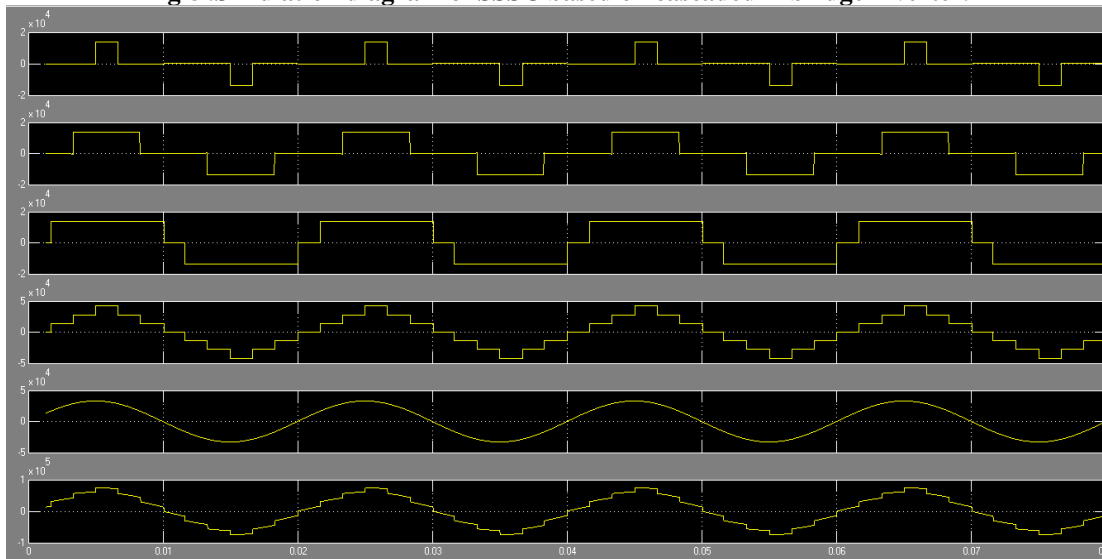
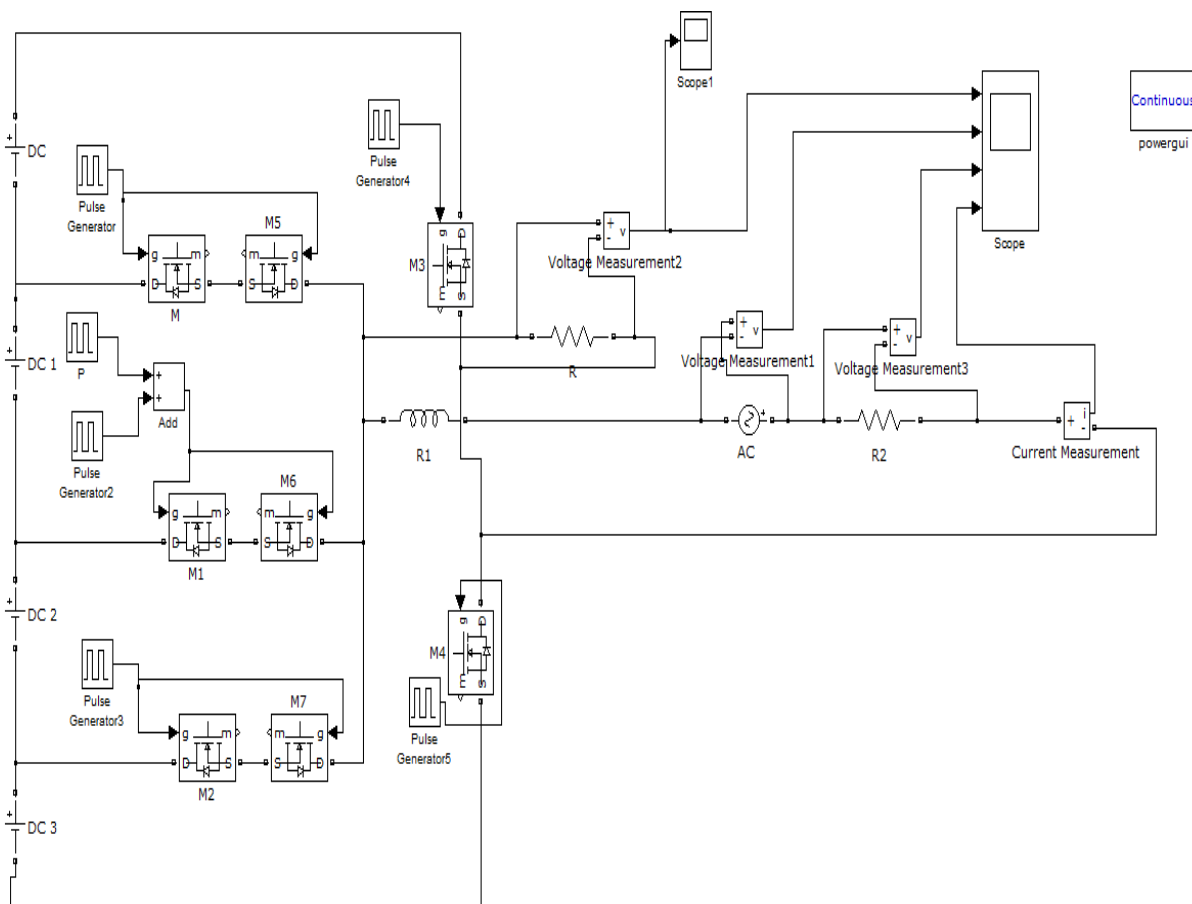
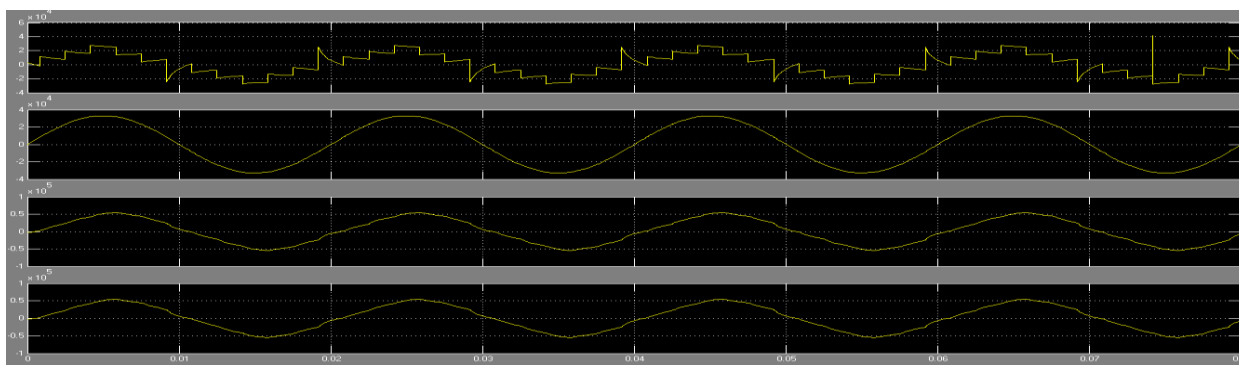


Fig 9. Output of fig 8 showing individual bridge voltages, inverter output, ac voltage, and combination of inverter and ac voltage.



**Fig10. Simulation diagram of SSSC based on the new inverter design.**



**Fig 11. Output of fig 10, showing inverter output, transmission voltage, Combination of both and transmission current**

By comparing the results of both the SSSC scheme it is clearly visible that the same results of conventional FACTS could achieve with the proposed scheme with less number of switches. In this paper the system is arranged in such a way that the injected voltage is in phase with the transmission line current. Thus this system is only doing active power compensation and it is not affecting the reactive power. But with a proper controller this system can be used for either active or reactive power compensation or for both. This proposed inverter can be used to generate different levels, with the addition or reduction of DC sources and switches.

### IX. CONCLUSION

The harmonic content of the single level facts systems are suppressed by using the multilevel facts systems. This paper gives a new inverter design for certain facts application which helps in reducing the switching losses and improvement of efficiency.

**REFERENCE**

- [1]. Ahmet Mete Vural , KamilCagatayBayindir Converter Level Modeling and Control of Quasi Multi-Pulse Static Synchronous Series Compensator, IEEE Symposium on Electrical & Electronics Engineering (EEESYM) 2012
- [2]. DipendraRai, Sherif O. Faried, G.Ramakrishna and Abdel-AtyEdris, "An SSSC-Based Hybrid Series Compensation Scheme Capable of Damping SubsynchronousResonance"IEEE transaction on power delivery, vol127, no.2, apri/2012.
- [3]. Mohammad Hassan Ameri, ShahrokhFarhangi, "A New Simple Method for Capacitors Voltage balancing in Cascaded H-bridge SSSC", Member, iEEE 2010
- [4]. L. Gyugyi." Power electronics in electric utilities: Static V AR compensators". Proceedings of the iEEE. vol176, no.4 pp.483- 493, Apr.1998
- [5]. Qiang Song, Wenham Liu, "DC Voltage Balancing Technique Using Multi-Pulse Optimal PWM for Cascade H-Bridge Inverters Based STATCOM", 35rh Annual iEEE Power Electronics Specialists Conference,2004
- [6]. M. Bongiorno,J. Svensson, and L. Ängquist, "Single-phase VSC based SSSC for subsynchronous resonance damping," iEEE Trans. Power Dei., vol. 23, no. 3, pp. 1544-1552,Jul. 2008.
- [7]. D. Rai, G. Ramakrishna, S. O. Faried, and A. Edris, "Enhancement of power system dynamics using a phase imbalanced series compensation scheme," iEEE Trans. Power Syst., vol. 25, no. 2, pp. 966--974, May 2010.
- [8]. D. Rai, S. O. Faried, G. Ramakrishna, and A. Edris, "Hybrid series compensation scheme capable of damping subsynchronous resonance,"Proc. inst. Eng. Technol. Gen., Transm. Dislrib., vol. 4, no. 3,pp. 456--466, March 2010.
- [9]. Chong Han, Alex Q. Huang , "A Generalized Control Strategy of Per-Phase DC Voltage Balancing for Cascaded Multilevel Converterbased STATCOM". PESC 2007, pp. I 746-1 752,2007
- [10]. Jon AndoniBarrena\_, Luis Marroyo, "A Novel PWM Modulation Strategy for DC Voltage Balancing in Cascaded H-Bridge Multilevel Converters" ,EUROCON 2007, pp.1450-1456, 2007
- [11]. J.A.Barrenal, S.Aurtenecheal,J. M. Canales'M. "Design, Analysis and Comparison of Multilevel Topologies for DSTATCOM Applications", EPE 2005